Robust CMOS Compatible Photonic Crystal Nanocavity and DEMUX Filter

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Various high Q microcavities

- Various microcavities
- Quality factor and mode volume
- Applications

Quality factor

\[ Q = \omega \times \frac{\text{stored energy}}{\text{power in/out}} \]

Photon density

\[ \propto \frac{Q}{V} \]

Applications

- All-optical switching
- Optical buffer
- Cavity QED devices
- Low-threshold lasers
- Optical sensors
- Optical frequency combs
Outline

1. Introduction
2. CMOS compatible high-Q cavity
   a. SiO$_2$ clad structure
   b. Photolithographic fabrication
3. Controlling randomness
4. EO modulator / pin receiver
5. DEMUX
6. Summary
Si photonics & Photonic crystal

### Si photonics

#### All-optical switch

- Low energy: 25 pJ
- Response time: ~450 ps

#### E/O modulator

- Conversion: E ↔ O
  - pn dope region
  - Speed: 12.5 Gbit/s

#### Ge epitaxial grown

- Detector at 1550 nm
- Speed: 31 GHz
- Responsivity: 1.16 A/W

### Photonic crystals

#### High-Q & low mode volume

- Enhance light & matter interaction

#### Raman laser

- Light source
  - \( Q = 9 \times 10^6 \)

### Problem

1. **Air-bridge structure**
   - Incompatible with Si photonics devices
Si photonics & Photonic crystal

Si photonics
CMOS-process
Photolithography

Integration

Voltage assisted light source

Photonic crystals
High-Q & low mode volume

\[ \frac{Q}{V} \]

Enhance light & matter interaction

Problem

2. EB lithography

Incompatible with Si photonics devices

Problem

2. EB lithography

Incompatible with Si photonics devices

Raman laser

Light source
\[ Q = 9 \times 10^6 \]
Motivation

Si-photonics

1. SiO₂-cladding
2. Photolithography

Photons crystals

Air-bridge

EB-lithography

Problems

This work has been opening the way of the future...

Fusion of

Si-photonics & Photonics crystals
Design & Simulation

Width-modulated line defect cavity

Principle of confinement

Optimized structure

Fabricated parameter

Photolithographic fabrication? & Dielectric cladding?

FDTD – w/ SiO₂ cladding


Optimized structure

Fabricated parameter

Q = 7.1 \times 10^6

V = 2.4 \left(\frac{\lambda}{n}\right)^3

Q = 8.1 \times 10^5

V = 1.7 \left(\frac{\lambda}{n}\right)^3

Q = 8.1 \times 10^5

V = 1.7 \left(\frac{\lambda}{n}\right)^3
Effect of photolithography

Fabrication error (SEM images)

Width-modulated line defect cavity

Max amount of shift: 9 nm

L3 cavity

Max amount of shift: 63 nm

-->

Width-modulated line defect cavity is robust against the proximity effect coming from photolithography.
Properties

Transmission spectrum

The highest $Q$ of PhCs demonstrated with photolithography

$Q = 2.2 \times 10^5$
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Effect of photolithography

Simulation including the deviation of hole diameter

![Graph showing the relationship between Q-factor and deviation of hole diameter.](image)
Managing the randomness

3. Controlling randomness

Design of our device

Waveguide width

W1.05 → wide
W0.98 → narrow

Cutoff frequency (mode gap)

Position of light localization occurs randomly in W0.98


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Managing the randomness

3. Controlling randomness


Design of our device

Waveguide width

W1.05 → wide
W0.98 → narrow

Cutoff frequency (mode gap)

Position of light localization
occurs only in W0.98

The effect of randomness occurs in a limited area (controlled way)
Regimes of randomness

- **Dispersive** \( l_c \gg L \)
- **Diffusive** \( l_c \approx L \)
- **Localized** \( l_c \ll L \) — Strong

**Calculation**

- Performed 18 times calculation
- 2 nm deviation to the diameter and position of PhC holes

**Experiment**

- 18 devices measured
- Setup:
  - TLD
  - PCWG
  - PM

Localization observed at desired position

\[ Q = 2.4 \times 10^5 \]
Yield rate of obtaining localization

Calculation

33% 56% 61% 67%

Experiment

28% 67% 61% 83%

> 80% yield obtained

Using random PhC for controlled experiment


EO modulation achieved w/ pin structure integrated at W0.98 regime

EO modulation achieved w/ pin structure integrated at W0.98 regime
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## EO modulator

<table>
<thead>
<tr>
<th>Fabrication process</th>
<th>Photolithography (easy)</th>
<th>EB Lithography (complicated)</th>
<th>Photolithography (easy)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Structure</td>
<td>Silica clad</td>
<td>Air-bridge</td>
<td>Silica clad</td>
</tr>
<tr>
<td>Size</td>
<td>400μm×500μm</td>
<td>10μm×5μm</td>
<td>10μm×5μm</td>
</tr>
<tr>
<td>Speed</td>
<td>10GHz</td>
<td>100MHz</td>
<td>100MHz</td>
</tr>
<tr>
<td>Voltage</td>
<td>5V</td>
<td>2V</td>
<td>2V</td>
</tr>
</tbody>
</table>


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Photo detection on silicon chip

**Ge on Si detector** $0.89 \sim 1.16 \text{ A/W}$

31GHz Ge $n-i-p$ waveguide photodetectors on Silicon-on-Insulator substrate

Tao Yin$^1$, Rami Cohen$^2$, Mike M. Morse$^1$, Gadi Sarid$^1$, Yoel Chetrit$^2$, Doron Rubin$^3$, and Mario J. Paniccia$^1$

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- Developed by a number of groups (Intel, IBM, MIT, Cornell, etc…)
- **Advantage:**
  - Very fast (>40 GHz)
  - High sensitivity (QE~80%)
- **Disadvantage**
  - Complicated fabrication
  - Large dark current due to defects

**Ion-implanted Si detector** $0.8 \text{ A/W}$

CMOS-Compatible All-Si High-Speed Waveguide Photodiodes With High Responsivity in Near-Infrared Communication Band


IEEE PHOTONICS TECHNOLOGY LETTERS, VOL. 19, NO. 3, FEBRUARY 1, 2007

- Developed by MIT
  - **Advantage:**
    - All-silicon = CMOS-Compatible
    - Good sensitivity and speed
  - **Disadvantage:**
    - Unstable (large aging effect)
    - Large dark current due to defects
Advantages of an all-silicon detector

Detect 1.5-μm telecom light using Si-chip integrated p-i-n diode

Advantages:

- Low dark current (because it is all-silicon)
- High sensitivity (due to the high-\( Q \) cavity)
- CMOS compatible fabrication
- Wavelength channel selective detector
Experimental result & calculation

 Numerical model

 Light energy $u$ stored in cavity

$$\frac{du}{dt} = \sqrt{T} P_{in} - \frac{u}{\tau_{ph}} - \sigma N \frac{c}{n} \frac{u}{n^2 V_m} - \frac{2c^2 \beta}{n^2 V_m} u^2$$

 Carrier density $N$

$$\frac{dN}{dt} = \frac{2c \beta \lambda}{h n^2 V_m^2} u^2 - \frac{N}{\tau_c} - \frac{I}{eV_m} + \frac{2\alpha \lambda}{h n V_m} u$$

 Carriers generated by OPA
 Carrier generation by TPA
 Energy loss by FCA

 Current vs. carrier density

$$I = e \mu \phi S \frac{N}{d}$$  (Einstein-Smoluchowski relation)

 Good agreement between experiment and calculation
 High efficiency confirmed by model calculation


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Dark (leak) current: Air-bridge PhC


Very low dark current (max. -15 pA @ -3 V)
Dark (leak) current: $\text{SiO}_2$ clad PhC nanocavity

![Graph showing photocurrent vs. bias voltage](image-url)
Responsivity of SiO$_2$ clad pin PhC nanocavity

![Responsivity graph](image)

- **Photocurrent (A)** vs **Input power (W)**
- **13.4 mA/W**
- **0.89 % at 0.3mW input power**

4. All-silicon pin receiver
## Comparison w/ other detectors

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Quant. eff.</th>
<th>Dark current</th>
<th>Min. detectable in. light power</th>
<th>Device length</th>
<th>Operation voltage</th>
<th>Operation reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si PhC (SiO₂ clad)</td>
<td>0.89%</td>
<td>12 pA</td>
<td>~100 nW</td>
<td>8.4 μm</td>
<td>-3 V</td>
<td>This work (2017)</td>
</tr>
<tr>
<td>Si PhC (AB)</td>
<td>9.7%</td>
<td>15 pA</td>
<td>0.9 nW</td>
<td>8.4 μm</td>
<td>-3 V</td>
<td>APL 96, 101103 (2010).</td>
</tr>
<tr>
<td>Ge on Si</td>
<td>71%</td>
<td>169 nA</td>
<td>~190 nW</td>
<td>50 μm</td>
<td>-2 V</td>
<td>Intel: OE 15, 13965 (2007).</td>
</tr>
<tr>
<td>Si⁺ implanted Si</td>
<td>~16%</td>
<td>0.5 nA</td>
<td>~2.5 nW</td>
<td>3~4 mm</td>
<td>-5 V</td>
<td>MIT: IEEE-PTL 18, 1882 (2006)</td>
</tr>
<tr>
<td>AlGaInAs-QW</td>
<td>~25%</td>
<td>~140 nA</td>
<td>~0.45 μW</td>
<td>~400 mm</td>
<td>-3 V</td>
<td>Intel: OE 15, 6044 (2007)</td>
</tr>
<tr>
<td>InGaAs</td>
<td>~80%</td>
<td>1.5 nA</td>
<td>~1.6 nW</td>
<td></td>
<td>-5 V</td>
<td>From brochure</td>
</tr>
</tbody>
</table>
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Principle of our DeMUX

Linear frequency tuning achieved by changing lattice constant

• Top view

• FDTD calculation
Photonic Structure Group, Keio University

PhC DeMUX filter fabricated w/ CMOS compatible process

- DeMUX design w/ tuning heater

- Fabricated DeMUX device


First demonstration of photolithographically fabricated photonic crystal DeMUX
In-plane 8ch DWDM demonstration

Setup

Eye pattern

1 GHz

(c)

2.5 GHz

5. DeMUX
We can achieve DeMUX with 64 channels with small crosstalk

FDTD calculation

- Transmittance of 32 channels DeMUX

- Transmittance of 64 channels DeMUX
# Discussions & Comparisons

First demonstration of photolithographically fabricated photonic crystal DeMUX

<table>
<thead>
<tr>
<th>Stability &amp; Structure</th>
<th>Fabrication method</th>
<th># of channels</th>
<th>Channel spacing</th>
<th>Configuration</th>
<th>Footprint</th>
<th>Other remarks</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>High &amp; PhC SiO₂ clad</td>
<td>Photo-lithography</td>
<td>8</td>
<td>267 GHz</td>
<td>In-plane</td>
<td>110 μm²</td>
<td>WM cavity</td>
<td>This work</td>
</tr>
<tr>
<td></td>
<td></td>
<td>14</td>
<td>131 GHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low &amp; PhC air-bridge</td>
<td>EB lithography</td>
<td>5</td>
<td>3.7 THz</td>
<td>In-plane</td>
<td>30 μm²</td>
<td>L3 cavity</td>
<td>OE 14, 12394 (2006)</td>
</tr>
<tr>
<td>Low &amp; PhC air-bridge</td>
<td>EB lithography</td>
<td>32</td>
<td>100 GHz</td>
<td>Out-of-plane</td>
<td>100 μm²</td>
<td>L3 cavity</td>
<td>OE 22, 4698 (2014)</td>
</tr>
<tr>
<td>High &amp; Si-AWG</td>
<td>Photo-lithography</td>
<td>8</td>
<td>250 GHz</td>
<td>In-plane</td>
<td>17000 μm²</td>
<td></td>
<td>OL38, 2961 (2013)</td>
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</table>


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Summary: Photonic crystal

1. CMOS compatible high-Q cavity
   a. Fabrication: Photolithography
   b. Structure: SiO2 clad structure

   Highest Q w/ CMOS compatible process/structure achieved (Q = 2.2 × 10^5)

2. Application of PhC nanocavity device
   a. All-silicon pin receiver: High sensitivity
   b. DeMUX filter: Very small size w/ ~100 GHz spacings

   Small dark current / small size / etc.
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The team

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