Improved CMOS compatible photonic crystal demultiplexer

Keio University  Graduate School of System Design and Management
Shengji Jin, Yuta Ooka, Tomohiro Tetsumoto, Nurul Daud,
Naotaka Kamioka, Taku Okamura, Takasumi Tanabe

kins@phot.elec.keio.ac.jp
Data traffic estimation (mobile and data center)

- Mobile data traffic estimation
- Data traffic estimation in data center

### Cisco Visual Networking Index 2017

- Twice in 2 years
- Middle East
- Africa
- Center & East
- Europe
- Latin America
- Asia
- EU
- North America

### Cisco Global Cloud Index 2017

- Rapid increase
- Within data center
- Between data center
- Data center - users
Shortening distance of optical telecom

Si photonics devices

Electric wiring vs. Optical wiring (Ultra short distance)

Wiring width+pitch width
- Cu ~100 nm
- Co ~100 nm
- CNT < 100 nm

Si: ~um
(400 nm width + >1 um pitch)

Bandwidth
- < 3 GHz
- > 10 GHz/ch

Capacity / 1um wiring width
- ~ 10 GHz
- < 10 GHz/ch

We need several channels to utilize advantages of optical wiring

Ultra compact DeMUX
# Characteristics of various DeMUX

<table>
<thead>
<tr>
<th>DeMUX devices</th>
<th>PLC (silica)</th>
<th>Si - AWG</th>
<th>Si - PhC</th>
</tr>
</thead>
<tbody>
<tr>
<td>[Image]</td>
<td>[Image]</td>
<td>[Image]</td>
<td>[Image]</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Fabrication method</th>
<th>PL</th>
<th>Photolithography</th>
<th>Photolithography</th>
<th>EB lithography</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of channel</td>
<td>400</td>
<td>512</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>Channel spacing (GHz)</td>
<td>25</td>
<td>25</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>Device size (µm²/ch)</td>
<td>2.0×10⁷</td>
<td>7.6×10⁴</td>
<td>1.0×10²</td>
<td></td>
</tr>
<tr>
<td>Productivity</td>
<td>⬤</td>
<td>△</td>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>

Y. Hida, et. al, OSA TOPS Vol. 54 Washington DC (2001)
Objective (Required properties of DeMUX)

I. Size: 100 μm² order

Ultra small size is ideal in terms of on-chip integration
→ PhC or plasmonic circuits

II. Number of channel: ~10 ch (@ ~10 Gb/s per. ch.)

Around 10 ch would be needed to utilize optical wiring’s advantages

III. Crosstalk: -10 dB ~ -20 dB

Our target is ultra-short distance and do not need EDFA
Around -20 dB would be enough

IV. Total loss: -10 dB

Micro strip line’s transmission loss: ~ -3 dB/cm
→ Around -10 dB loss@electrical@distance: ~ cm
Optical wiring’s loss: - 0.2 dB/cm → input loss is bigger

V. Others: Mass production(Photolithography)・Stability(SiO₂ cladding・heaters)

PhC DeMUX made by photolithography
CMOS compatible high Q PhC cavity

- High Q cavity
- Photolithography
- SiO₂ cladding

```
Q = 2.2 \times 10^5
```
Design of DeMUX consisting of PhC cavity


- Design / upper view
- FDTD simulation

- Changing lattice constant linearly
  - lattice constant: 420 nm ~ 413 nm
  - Number of channel: 8 ch
Fabrication of CMOS compatible DeMUX

- Fabrication
  - CMOS process foundry (IME in Singapore)
  - 248-nm lithography (with phase-shifting mask)
- Device
- Transmission property (1Gbps/2.5Gbps)
Objective (Required properties of DeMUX)

I. **Size**: 100 μm² order
   - Ultra small size is ideal in terms of on-chip integration → PhC or plasmonic circuits

II. **Number of channel**: ~10 ch (≈ 10 Gb/s per. ch)
   - Around 10 ch would be needed to utilize optical wiring’s advantages

III. **Crosstalk**: -10 dB ~ -20 dB
   - Our target is ultra-short distance and do not need EDFA
     - Around -20 dB would be enough

IV. **Total loss**: -10 dB
   - Micro strip line’s transmission loss: ~ -3 dB/cm
     - Around -10 dB loss @ electrical distance: ~1 cm
   - Optical wiring’s loss: -0.2 dB/cm → input loss is bigger

**Drawbacks**:
- Mass production (Photolithography) • Stability (SiO₂ cladding • heaters)
- Fluctuation (-16 dB) • Big loss (-30 dB)

PhC DeMUX made by photolithography
Cause of crosstalk

- Undesirable crosstalk

Experiment

- Influence of mode edge

W0.98 mode edge

Resonance

Problem: Mode edge may couple to PhC cavity

Wavelength

FDTD simulation

Transmittance (a.u.)

Transmittance (dBm)

Wavelength (nm)

1555 1560 1565 1570

1550 1555 1560 1565 1570 1575

1550 1555 1560 1565 1570 1575

10^0 10^-1 10^-2 10^-3 10^-4

1550 1555 1560 1565 1570 1575

10^0 10^-1 10^-2 10^-3 10^-4

1550 1555 1560 1565 1570 1575

(a)

BUS WG

Coupling

ch8 \( a = 413 \text{ nm} \)

ch1 \( a = 420 \text{ nm} \)
Optimization of output waveguides’ position

- **Position of output WG**
  - y
  - +3
  - +2
  - +1
  - 0
  - -1
  - -2
  - 0 +1 +2 +3 +4 +5

- **FDTD simulation (Optimized results)**
  - (x,y)=(0,0)
  - (x,y)=(3,0)

- **Basic strategy for optimization**
  - Suppress the undesirable peak caused by mode edge
Improved crosstalk and transmittance

➢ (i) Crosstalk (Simulation)

➢ (ii) Transmittance (Simulation)

➢ (i) Crosstalk (Experiments)

➢ (ii) Transmittance (Experiments)
Measured spectrum

Before improvement (0,0)

After improvement (3,0)

<table>
<thead>
<tr>
<th></th>
<th>Before improvement (0,0)</th>
<th>After improvement (3,0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total loss (dB)</td>
<td>35～40</td>
<td>15～20</td>
</tr>
<tr>
<td>Crosstalk (dB)</td>
<td>−8.36</td>
<td>−29.3</td>
</tr>
<tr>
<td>Fluctuation (dB)</td>
<td>16.2</td>
<td>5.5</td>
</tr>
</tbody>
</table>

Y. Ooka, Master thesis, 2017
Objective (Required properties of DeMUX)

I. **Size**: 100 μm² order

Ultra small size is ideal in terms of on-chip integration → PhC or plasmonic circuits

II. **Number of channel**: ~10 ch (@ ~10 Gb/s per. ch.)

Around 10 ch would be needed to utilize optical wiring's advantages

III. **Crosstalk**: -10 dB ~ -20 dB

Our target is ultra-short distance and do not need EDFA. Around -20 dB would be enough

IV. **Total loss**: -10 dB

Micro strip line’s transmission loss: ~ -3 dB/cm → Around -10 dB loss at electrical distance: ~ cm

Optical wiring’s loss: ~ -0.2 dB/cm → input loss is bigger

**Others**: Mass production (Photolithography) • Stability (SiO₂ cladding • heaters)

PhC DeMUX made by photolithography

Is it really possible to realize 100 μm² order?

How about influence of adjacent heaters?
Optimization of device size (heater interval)

➢ Heat-flux simulation (COMSOL)

Power: 40 mW

✓ Optimum heater interval
  9.5 μm

✓ Optimum size
  110 μm²/ch
Conclusion

- We achieve crosstalk of $-29.3 \text{ dB}$
- We could improve total loss form $35 \text{ dB}$ to $15 \text{ dB}$
- We optimize the device size to $110 \mu m^2/\text{ch}$ through heat-flux simulation

<table>
<thead>
<tr>
<th>Fabrication method</th>
<th>Photolithography</th>
<th>EB lithography</th>
<th>Photolithography</th>
<th>Photolithography</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of channel</td>
<td>8</td>
<td>32</td>
<td>512</td>
<td>400</td>
</tr>
<tr>
<td>Channel spacing (GHz)</td>
<td>240</td>
<td>100</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>Device size ($\mu m^2/\text{ch}$)</td>
<td>110</td>
<td>100</td>
<td>76000</td>
<td>20000000</td>
</tr>
<tr>
<td>Crosstalk (dB)</td>
<td>$-29$</td>
<td>$-$</td>
<td>$-4$</td>
<td>$-20$</td>
</tr>
</tbody>
</table>
Thanks for listening

Strategic Information and Communications R&D Promotion Programme (SCOPE), from the Ministry of Internal Affairs and Communications