Robustness of scalable all-optical NAND gate

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We designed scalable all-optical logic gates based on microrings that operate at the same input and output wavelengths. We investigated the influence of input power fluctuations and fabrication errors.

Key words: Photonic integrated circuits; Microring resonator; Coupling mode theory.

1. Introduction

Recent progress on ultrahigh-Q microcavities has enabled us to develop an all-optical logic gate on a chip that operates at ultralow power [1]. Several groups have demonstrated logic operations numerically [1], but experimental implementation has remained a challenge. There are certain criteria that a system must satisfy. First, the input and output signals must have the same wavelength; otherwise it is extremely difficult to connect systems in tandem. Secondly, it is preferable to construct the system with one cavity design, because the fabrication will then be easier. Although we can use an ideal structure in a simulation, in practice there are fabrication errors and power fluctuations.

2. Basic elements of logic gates

We use silicon nitride (Si3N4) microring resonators because they can employ the optical Kerr effect thanks to the large bandgap of the material. The cross-section of the air-clad waveguide is 900 nm wide and 600 nm high. Figure 2 is a schematic illustration of the microcavity. The radius of the ring resonator R is 20 μm; hence the mode volume V of the cavity is 1.5×102 μm3. The linear and nonlinear refractive indexes are n0 = 1.98, and n2 = 2.5×10-15 cm2W-1, respectively. We assume the cavity resonates at 1550 and 1580 nm. The unloaded quality factor (Qunload) for both resonant modes is 1.0×106, and this value is given by Q = ω0τloss, where ω0 is the resonant angular frequency of the cavity and τloss is the loss rate towards the outside. The input wavelengths are slightly detuned from the resonance and are set at λ1 = 1550.01 nm and λ2 = 1550.02 nm.

3. Designs of all-optical logic circuits

First we design a NAND gate, since it is a basic element of logic gates. The photonic circuit is shown in Fig 2(a), and is made of five cavities denoted C1, C2, C3, C4, and C5, which had τcoup values set at 150, 100, 250, 250, and 100 ps, respectively. C1 and C3 switch the signals on and off, and thus contribute directly to the logic operation. C4 is used to switch between λ2 and λ1. C2 and C5 are used to filter out unnecessary drive light.

Fig. 1: Operating principle of Kerr switching.

Figure 1 shows an example switching operation in an add-drop ring resonator system, where one wavelength is used as a signal and the other as a control. Throughout this study, we use coupled mode theory (CMT) [2] to analyze the logic gate operations.
wavelengths to drive the system; but as discussed previously, this does not degrade system scalability.
Pulsed drive sources with an amplitude of 360 mW are applied with a cycle of 5 ns and a duty ratio of 60%.

Figure 2(b) shows the calculated output waveform when inputs 1 and 2 are applied as shown in the graph. First, we set high input 1 (ON) and low input 2 (OFF) from 0 to 3 ns. The output exhibits a high state. When we switch both inputs to a high state (from 5 to 8 ns), the output is in a low state. We obtained a low state only when inputs 1 and 2 are both high, and this corresponds to a NAND gate operation.

4. Input power fluctuations

We investigated the system tolerance to input power fluctuations by calculating the output amplitude with different input powers. We set the drive light power at 360 mW, and changed the amplitude of the input signal. Figure 3 shows the input and output characteristics for four different gates. The black square dots show when we set the powers of inputs 1 and 2 at the same value and changed both powers simultaneously. The red circular dots indicate the output amplitude when we fixed input 2 amplitude at 250 mW and changed input 1. The blue triangles show the result we obtained when we fixed input 1 at 250 mW and changed the power of input 2.

Figure 3(a) and (b) show the output amplitudes for AND and OR gates. The output of an AND gate is at a low state when one of the inputs (1 or 2) is less than 60 mW. The output signal rises when the input exceeds 100 mW. The output is unstable when the input is between 60 and 100 mW. When we set the output power threshold at 50 mW, we need an input larger than 170 mW. However, if we increase the input too much, the output amplitude decreases again. This is due to the supply of excess light to the C4 cavity of the AND gate. This analysis reveals that the optimized input is in the 160 to 300 mW range for a high input and from 0 to 50 mW for a low input. This tolerable power range is sufficiently large for practical use.

Figure 3(c) shows the NOR gate output. The output is low only when inputs 1 and 2 are at a low state. The graph shows that this gate is at a low state when both inputs are less than 80 mW. When the input increases to 300 mW, the output amplitude rises. As a result of this analysis, we found that the input power for this NAND gate must set in the 230 to 400 mW range for a high input and at less than 50 mW for a low input.

The results for all the gates show that the upper limit of the OFF signal is 40 mW and is restricted by the OR gate, and the lower limit of the ON signal is 290 mW and is restricted by the NAND gate, when we set the output threshold value at 50 mW. Through this study, we found that the input power fluctuations are not a critical issue in our system.

5. Resonant wavelength fluctuations

Next, we investigated the effect of the resonant wavelength fluctuation of cavities. Resonant wavelength fluctuations occur as a result of imperfect fabrication. Our system uses 4 (or 5) cavities, and each cavity has two resonant modes. To investigate the effect of the presence of wavelength fluctuation, we added random fluctuations to all the 8 (or 10) resonant modes. Wavelength fluctuations are added based on a normal distribution, and their widths are characterized by standard deviation $\sigma$. We calculated the output with CMT, and determined whether or not the system had failed. Table 1 summarizes the result for NAND and other gates. $\sigma_{\text{lim}}$ is the standard deviation that reaches an error rate of 50%. $S_{\text{max}}$ is the full width at half maximum (FWHM) of the resonant spectrum of the cavity with the lowest loaded $Q$ used in the system. $S_{\text{min}}$ is the FWHM of the spectrum of the cavity with the highest loaded $Q$ used in the system. From the result, we know that the NAND gate is the most sensitive of all types. The allowed fluctuation is about 0.3 of the cavity width. Although fluctuation where $\sigma < 3.0$ pm is not easy...
to achieve, this value can be improved by designing a system where the cavities couple more strongly with the waveguides.

Table 1. Maximum and minimum widths of resonant spectrum (FWHM) $S_{\text{max}}$, $S_{\text{min}}$, and the standard deviation $\sigma_{\text{lim}}$ limit of each logic gate

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<th>OR</th>
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<tr>
<td>$S_{\text{max}}$</td>
<td>17.0 pm</td>
<td>17.0 pm</td>
<td>17.0 pm</td>
<td>26.0 pm</td>
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<tr>
<td>$S_{\text{min}}$</td>
<td>8.2 pm</td>
<td>10.0 pm</td>
<td>10.0 pm</td>
<td>10.0 pm</td>
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<tr>
<td>$2\sigma_{\text{lim}}$</td>
<td>6.0 pm</td>
<td>4.0 pm</td>
<td>7.0 pm</td>
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6. Gap distance fluctuations

Fabrication error causes both resonant wavelength fluctuations and fluctuations in the cavity-waveguide coupling, because the coupling $Q$ is determined by the gap distance $s$ between the cavity and the waveguide. To simplify this formulation, we assumed that the waveguide width $w$, refractive index $n$, and propagation constant $\beta$ are the same for the cavity and the waveguides. The transverse propagation constant $k_x$ and the evanescent field decay constant $\alpha$ in the cladding are given as

$$k_x = \sqrt{n^2k^2 - \beta^2}$$  \hspace{1cm} (1)

$$\alpha = \sqrt{\beta^2 - n^2k^2}$$  \hspace{1cm} (2)

where $k$ is the wave vector in a vacuum. From Eq. (1) and (2), the mode power $P$ is given as

$$P = \frac{\beta}{2\omega\varepsilon_0} \left(1 + \frac{1}{\alpha}\right)$$  \hspace{1cm} (3)

where $\omega$ is the angular frequency of the light and $\varepsilon_0$ is the vacuum permittivity. An expression for the coupling coefficient $\kappa$ between a straight waveguide and a curved waveguide (microring) is derived as,

$$\kappa = \frac{\omega_0}{2(2\alpha^2 + k_x^2)(n^2 - n_0^2)} \times \frac{\pi R}{\alpha} \exp(\alpha s)$$

$$\times \left[\alpha \cos\left(\frac{k_xw}{2}\right) \sinh\left(\frac{\alpha w}{2}\right) + k_x \sin\left(\frac{k_xw}{2}\right) \cosh\left(\frac{\alpha w}{2}\right)\right]$$  \hspace{1cm} (4)

where $\omega_0$ is the vacuum permittivity. $\tau_{\text{coup}}$ is given as,

$$\tau_{\text{coup}} = \frac{Q}{\omega} = \frac{\pi R n_e}{c k^2}$$  \hspace{1cm} (5)

where $n_e$ is the effective refractive index. We need to set the gap distance $s$ at 556, 588, 612, 630, and 644 nm to obtain $\tau_{\text{coup}}$ of 100, 150, 200, 250, and 300 ps, respectively, and these values are used in our logic gate designs. Now we can directly obtain $\tau_{\text{coup}}$ from $s$ hence we can study the impact of the imperfect fabrication of the gap distance $s$ with CMT analysis. In a similar way to that described in the previous section, we added a random error following the normal distribution $\sigma$ to all of the gaps.

Table 2 summarizes the results for different logic gates. Again the NAND gate is the most sensitive to the error. However, it is possible to achieve fabrication precision of better than $\pm12$ nm with current state-of-the-art fabrication technology.

Table 2. The limit of the fabrication fluctuation (in standard deviation $\sigma_{\text{lim}}$) for different logic gate

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<tbody>
<tr>
<td>$\sigma_{\text{lim}}$</td>
<td>22 nm</td>
<td>25 nm</td>
<td>40 nm</td>
<td>12 nm</td>
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7. Summary

We designed all-optical logic gates that operated at the same input and output wavelengths, which makes these logic gates highly scalable and easier to implement in practical use. We demonstrated their operation using coupled mode theory, and investigated various error tolerances. The upper limit of the OFF signal was 40 mW and the lower limit of the ON signal was 200 mW for our logic gate, whose power range is sufficiently robust for practical use. We found that the system was error-free when the device was fabricated with $\pm5$ nm precision and the error rate increased to 50% when the fabrication precision was $\pm12$ nm. In addition, we found that the sensitive dependence on the resonant wavelength fluctuation is critical. The error rate increased to 50% when the resonant wavelength fluctuated 3 pm.

We are attempting to increase the scalability of the system, and this is the first detailed theoretical study of the impact of fabrication error on the operation of such all-optical logic gates, which provides important information that will make it possible to build a bridge between numerical and practical studies.

References